

# A 2.45GHz Fully-Differential CMOS Image-Reject Mixer for Bluetooth Application

Pradeep B. Khannur,<sup>1</sup> Koh Soo Ling

Institute of Microelectronics (IME), 11 Science Park Road, Singapore Science Park II, Singapore 117 685; <sup>1</sup>Oki Techno Centre, Singapore (OTCS)

**Abstract** The design of a 2.45GHz image-reject mixer (IRM) for Bluetooth application using low-cost 0.35um, double-poly four-metal standard CMOS process with the metal-insulator-metal (MIM) capacitor option is described. The proposed design uses Hartley architecture with temperature compensation to significantly reduce the gain variation with temperature (-40°C to +85°C). In-house extracted models were used for active and passive components to achieve image rejection ratio (IRR) better than 45dB, input referred third-order intercept point (IIP3) better than -7dBm, voltage conversion gain better than 20dB and noise figure less than 20dB under all process, temperature, and voltage supply conditions. The intermediate frequency (IF) is 2MHz. The circuit operates from a 3V±10% supply and draws 10.4mA.

## I. INTRODUCTION

In all heterodyne including low-IF RF receivers a major problem is suppressing the interfering image frequency component. As shown in Fig.1 [1] the incoming wanted RF signal and unwanted image signal are converted to the same fixed IF. So, to filter out the image signal we have to use high-Q image-reject filter between low noise amplifier (LNA) and mixer. Otherwise, the image signal may corrupt the wanted RF signal and it may not be possible to recover the wanted data at all.

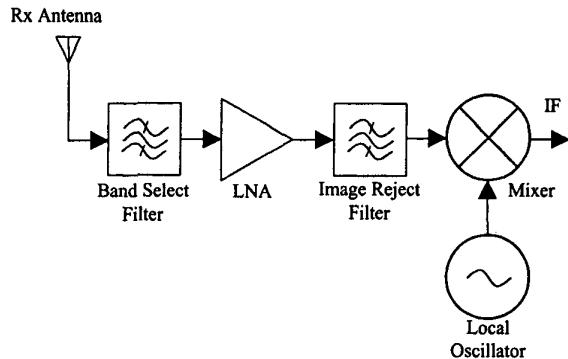


Fig. 1. Typical block diagram of heterodyne receiver

The disadvantages of using external image-reject filter are increased cost, increased board area, reduced reliability and increased weight. Also, if the IF is very low the image-reject filter cannot be realized even with SAW devices. In such cases one cost effective and practical way of rejecting image signal is to use IRM.

Bluetooth enabled devices have to be low-cost and light weight. It means need for full integration and low-cost process which is none other than CMOS. But CMOS has the following disadvantages: the variation of device and circuit parameters substantially degrade the performance at the extremes of process and temperature conditions, present day MOS device models appear quite inadequate for RF circuit simulations [1]. In this paper these problems are overcome by using in-house accurately extracted models and special design techniques such as temperature compensation circuit to reduce gain variation with temperature.

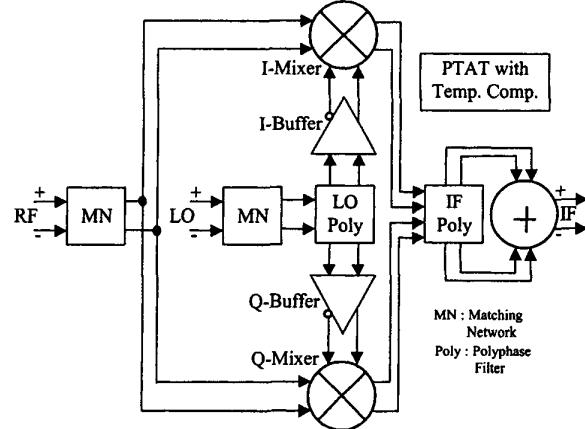


Fig. 2. Block diagram of image-reject mixer

The image-reject mixer is realized as per the block diagram [2] shown in Fig. 2. The image-rejection depends on the amplitude and phase imbalance at the input of the IF polyphase as given below [3]:

$$IRR = -10 \log \left[ \frac{1 - 2\sqrt{G \cos(\theta)} + G}{1 + \sqrt{G \cos(\theta)} + G} \right]$$

where  $IRR$  is image-rejection ratio in dB  
 $G$  is the gain imbalance (a ratio) and  
 $\theta$  is the phase imbalance in degree.

## II. CIRCUIT IMPLEMENTATION

As illustrated in Fig. 2 the proposed design uses Hartley architecture whose principle disadvantage is its sensitiveness to matching. This problem gets still worse with a low-cost CMOS process. These problems are overcome by using fully-differential architecture which makes IRM insensitive to noise coupling through the substrate; common-centroid layout technique for matching transistors, resistors, and capacitors; temperature compensation circuit for reducing gain variation with temperature. Also in-house extracted models for active and passive devices including parasitics such as transmission lines, package parasitics, etc. were used.

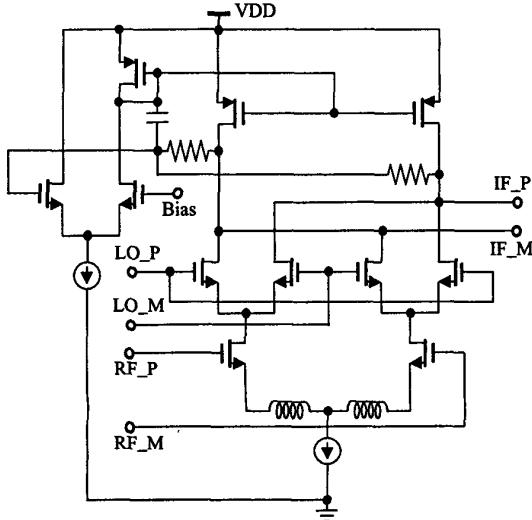


Fig. 3. Gilbert-cell mixer with CMFB

Fig. 3 shows the circuit diagram of double-balanced Gilbert-cell mixer with common mode feed back (CMFB). The Gilbert-cell mixer is optimally designed to achieve high linearity, low noise figure, and high voltage conversion gain. Active-load is used at the output to achieve higher conversion gain. Higher conversion gain is necessary to overcome the losses in the subsequent three stage IF polyphase network. The voltage gain at the drain of the switching core is set by CMFB such that necessary voltage swing is available at the IF output. The CMFB

also provides the gate biasing for the active load. The required linearity is achieved by using on-chip circular spiral inductors at the source of RF input transistors at the expense of a couple of dB in noise figure, which is not a stringent requirement for Bluetooth. Since the channel resistance contributes to the mixer noise performance the larger the MOSFET size, the lesser the noise contribution will be from the switching core. Larger devices add more parasitic capacitances and decreases the isolation. The MOSFET sizes are optimized to achieve required isolation. The differential RF input is injected into the lower pair of the mixer. The gate bias for the RF transconductance and local oscillator (LO) switching core is taken from proportional-to-absolute-temperature (PTAT) with temperature compensation for reducing gain variation with temperature.

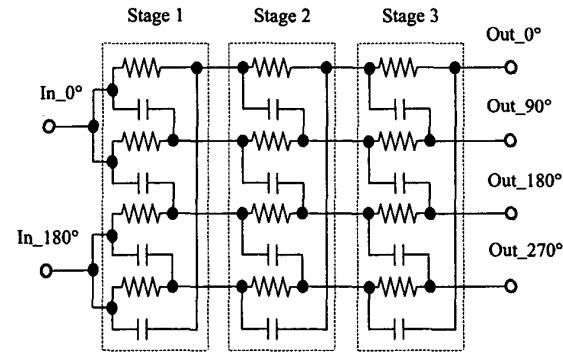


Fig. 4. LO polyphase schematic

The quadrature local oscillator signals are generated using three stage LO polyphase network as shown in Fig. 4. The poles of the three stages are set at 2.45GHz, 2.45GHz+20%, and 2.45GHz-20% to cater for resistor and capacitor tolerances in the fabrication. In the layout extreme care is taken to match the polyphase filter elements to achieve required amplitude and phase matching. All the resistors and capacitors in one stage are layed out in the same orientation. To balance contributions of line resistance, the interconnect lengths are made equal. All the capacitors used in the network are MIM capacitors between top two metals. This reduces the effect of substrate loss.

The IF polyphase network is similar to the LO polyphase network except that the poles are set at 2MHz, 2MHz+20%, and 2MHz-20%.

Fig. 5 shows the LO buffer schematic. It amplifies the input from the VCO after passing through LO polyphase such that the double-balanced mixer is operated near the LO power saturation point. This ensures that the

conversion gain of the mixer does not vary significantly with the variations in the LO power.

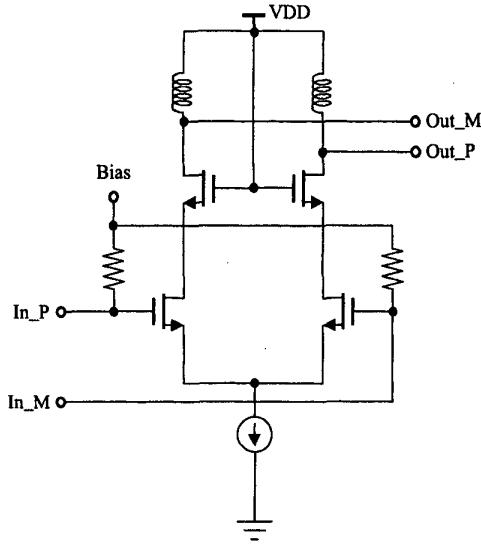


Fig. 5. LO buffer circuit

As shown in Fig. 6 the IF combiner is realized by two differential amplifiers which adds the quadrature components of the differential outputs from the IF polyphase network. The gate of the combiner is biased

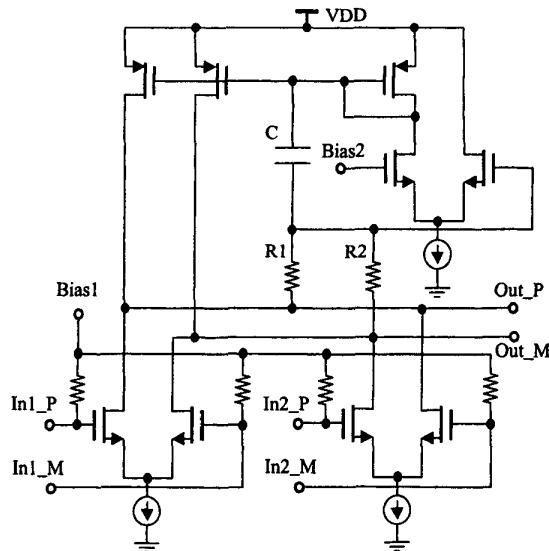


Fig. 6. IF combiner with CMFB

from PTAT. Active load is used to achieve higher gain. The CMFB circuit used is similar to the one used in double-balanced Gilbert-cell mixer. The CMFB provides the gate biasing of the active load.

Power-down feature is incorporated in the presented IRM to save power in sleep mode. IRM draws less than 2nA in power-down mode.

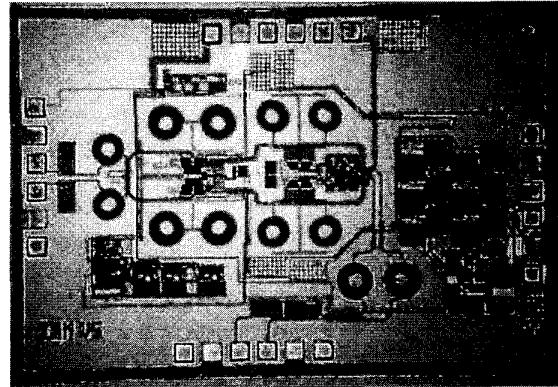


Fig. 7. Chip micrograph

The PTAT establishes stable reference voltages over temperature range  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Also temperature compensation circuit further reduces the gain and noise figure variation over this temperature range. The temperature compensation circuit consists of the following blocks: current comparator, temperature independent current reference, PTAT voltage reference circuit, temperature independent voltage reference, and PTAT current-to-voltage converter.

### III. EXPERIMENTAL RESULTS

A chip-micrograph is shown in Fig. 7. The IRM was packaged in a 24-pin QFP package and evaluated using FR-4 test PCB. Discrete RF baluns were used for feeding differential RF and LO signals to the IRM. In-house extracted package model and printed circuit board parasitics are included in the simulation. The performance of IRM exceeds the requirement of 2MHz IF Bluetooth receiver. As shown in the Fig. 8 there is very close match between simulated and measured voltage gain. Fig. 9 gives voltage gain vs. temperature with and without temperature compensation circuit. The measured image-rejection ratio is nearly 50dB at 2MHz IF as shown in Fig. 10. Table 1 below shows the measured results.

TABLE 1  
PERFORMANCE SUMMARY

Parameter	Measured Results
Operating voltage	3V $\pm$ 10%
Current drawn	10.4mA
Operating temperature range	-40°C to +85°C
Image-rejection ratio	> 45 dB
Voltage Conversion Gain	23.7 dB
Noise Figure	< 20 dB
IIP3 (dBm)	> -7 dBm

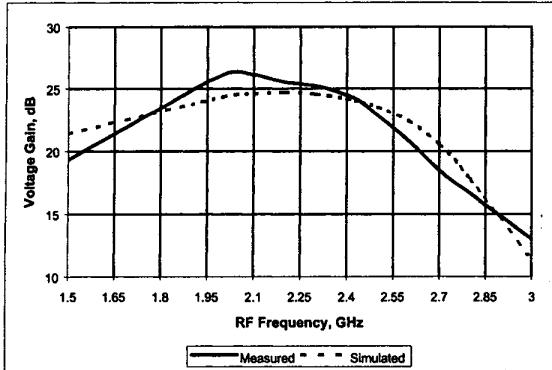


Fig. 8. Voltage gain versus RF frequency

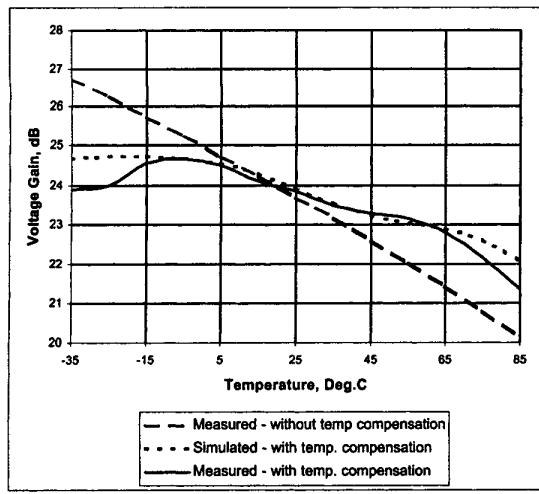


Fig. 9. Voltage gain versus temperature

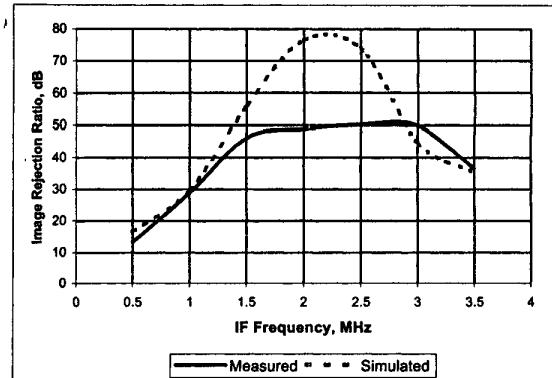


Fig. 10. Image-rejection ratio versus temperature

#### IV. CONCLUSION

The performance of the presented image-reject mixer exceeds the requirements for the Bluetooth receiver. With the use of temperature compensation circuit the gain variation with temperature has been improved from 6.8dB to less than 3dB over temperature range of -40°C to +85°C. The image rejection ratio of better than 45dB is achieved under all process, temperature, and voltage supply conditions. The noise figure is less than 20dB.

#### ACKNOWLEDGEMENTS

The authors gratefully thank the reviewers Aruna B. Ajjikuttira, Uday Dasgupta, Rajinder Singh, S.C. Rustagi of IME and Masaaki Itoh of OTCS, whose useful comments have been noted. They would also like to thank S. Chu of Chartered Semiconductor Manufacturing for process-related discussions. Thanks are also due to Moe Moe Aung, Boon Hwee Oh and Siao Peck Yong for their assistance. The contributions of Low Eng Chuan, Mark Choke, and Hiroshi Nakamura are acknowledged.

#### REFERENCES

- [1] Behzad Razavi, "Architectures and Circuits for RF CMOS Receivers" IEEE *Custom Integrated Circuits Conference*, pp 393-400, 1998.
- [2] Aruna Ajjikuttira, et al., "A Fully-Integrated CMOS RFIC for Bluetooth Applications," ISSCC Digest of Technical Papers, pp. 198-199, Feb. 2001
- [3] Lawrence E. Larson, *RF and Microwave Circuit Design for Wireless Communications*, Artech House, 1996